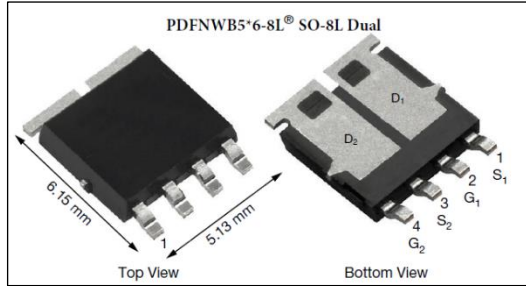




PDFNWB5×6-8L Plastic-Encapsulate MOSFETS

CCM2E30D04T N- and P-Channel Power MOSFET

PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
V _{DS} (V)	40	-40
R _{DS(on)} (mΩ) at V _{GS} = ± 10 V	7.5	26
R _{DS(on)} (mΩ) at V _{GS} = ± 4.5 V	9.5	38
I _D (A)	30	-30
Configuration	N- and P-Pair	



DESCRIPTION

The CCM2E30D04T provides excellent R_{DS(ON)} with low gate charge.

It can be used in a wide variety of applications.

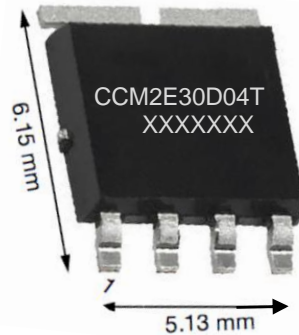
FEATURES

- TrenchFET® Power MOSFET
- AEC-Q101 Qualified^d
- 100 % R_g and UIS Tested

APPLICATIONS

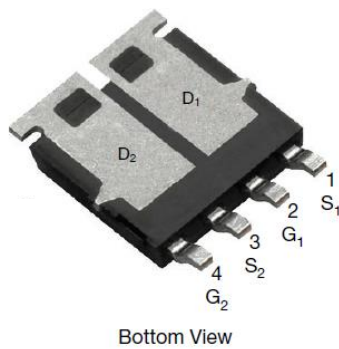
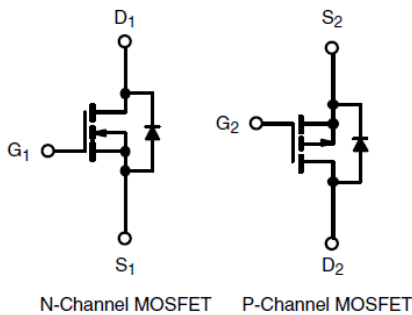
- Solenoid valve drive
- High-frequency switching

MARKING



CCM2E30D04T = PART NUMBER
 CCM= Cloudchild mosfet
 2=2PCS MOSFET
 E=Packing form
 30= ID30A; D=N+P MOSFET; 04=Bvds 40V;
 T= Trench
 XXXX= manufacture year week;
 XXX= N Mosfet wafer LOT NUM

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT	
Drain-Source Voltage	V _{DS}	40	-40	V	
Gate-Source Voltage	V _{GS}	± 20			
Continuous Drain Current ^a	T _C = 25 °C	I _D	30	-30	A
	T _C = 125 °C	I _D	30	-20	
Continuous Source Current (Diode Conduction) ^a	I _S	30	-30		
Pulsed Drain Current ^b	I _{DM}	120	-120		
Single Pulse Avalanche Current	L = 0.5 mH	I _{AS}	12	-11.5	mJ
Single Pulse Avalanche Energy		E _{AS}	36	33	
Maximum Power Dissipation ^b	T _C = 25 °C	P _D	48	48	W
	T _C = 125 °C		16	16	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175			°C
Soldering Recommendations (Peak Temperature) ^f		260			

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT	
Junction-to-Ambient	PCB Mount ^c	R _{thJA}	85	85	°C/W
Junction-to-Case (Drain)		R _{thJC}	3.1	3.1	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

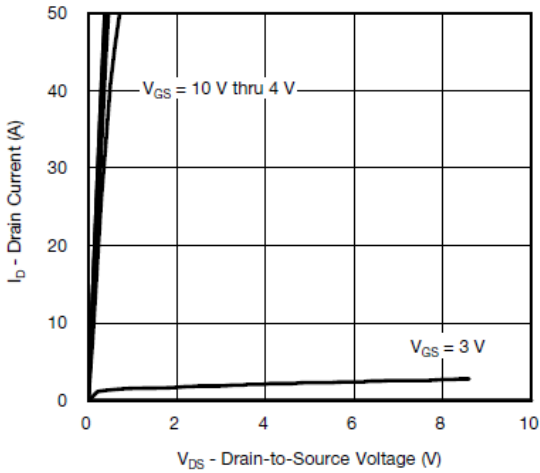
SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		N-Ch	40	-	V
		V _{GS} = 0 V, I _D = -250 μA		P-Ch	-40	-	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		N-Ch	1.0	1.5	3.0
		V _{DS} = V _{GS} , I _D = -250 μA		P-Ch	-1.1	-1.6	-2.2
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		N-Ch	-	-	± 100
				P-Ch	-	-	± 100
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V	N-Ch	-	-	1
		V _{GS} = 0 V	V _{DS} = -40 V	P-Ch	-	-	-1
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	N-Ch	-	-	50
		V _{GS} = 0 V	V _{DS} = -40 V, T _J = 125 °C	P-Ch	-	-	-50
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	N-Ch	-	-	150
		V _{GS} = 0 V	V _{DS} = -40 V, T _J = 175 °C	P-Ch	-	-	-150
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	N-Ch	25	-	-
		V _{GS} = -10 V	V _{DS} ≤ 5 V	P-Ch	-25	-	-
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	ID = 10 A	N-Ch	-	7.5	8.5
		V _{GS} = -10 V	ID = -10 A	P-Ch	-	26	33
		V _{GS} = 10 V	ID = 10 A, T _J = 125 °C	N-Ch	-	-	13.4
		V _{GS} = -10 V	ID = -10 A, T _J = 125 °C	P-Ch	-	-	37
		V _{GS} = 10 V	ID = 10 A, T _J = 175 °C	N-Ch	-	-	17
		V _{GS} = -10 V	ID = -10 A, T _J = 175 °C	P-Ch	-	-	45
		V _{GS} = 4.5 V	ID = 10 A	N-Ch	-	9.5	12.3
		V _{GS} = -4.5 V	ID = -10 A	P-Ch	-	37	42
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, ID = 10 A		N-Ch	-	65	-
		V _{DS} = -15 V, ID = -10 A		P-Ch	-	16	-
Dynamic^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch	-	1474	1843
		V _{GS} = 0 V	V _{DS} = -20 V, f = 1 MHz	P-Ch	-	1302	1628
Output Capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch	-	218	273
		V _{GS} = 0 V	V _{DS} = -20 V, f = 1 MHz	P-Ch	-	222	278
Reverse Transfer Capacitance	C _{rss}	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch	-	89	111
		V _{GS} = 0 V	V _{DS} = -20 V, f = 1 MHz	P-Ch	-	154	193

Total Gate Charge ^c	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 10\text{ A}$	N-Ch	25.5	38.3	nC		
		$V_{GS} = -10\text{ V}$	$V_{DS} = -20\text{ V}, I_D = -10\text{ A}$	P-Ch	30.2	45			
Gate-Source Charge ^c	Q_{gs}	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 10\text{ A}$	N-Ch	4.4	-			
		$V_{GS} = -10\text{ V}$	$V_{DS} = -20\text{ V}, I_D = -10\text{ A}$	P-Ch	4.1	-			
Gate-Drain Charge ^c	Q_{gd}	$V_{GS} = 10\text{ V}$	$V_{DS} = 20\text{ V}, I_D = 10\text{ A}$	N-Ch	4.3	-			
		$V_{GS} = -10\text{ V}$	$V_{DS} = -20\text{ V}, I_D = -10\text{ A}$	P-Ch	7.4	-			
Gate Resistance	R_g	$f = 1\text{ MHz}$			N-Ch	0.65	1.37	2.1	Ω
					P-Ch	3.1	6.15	9.5	

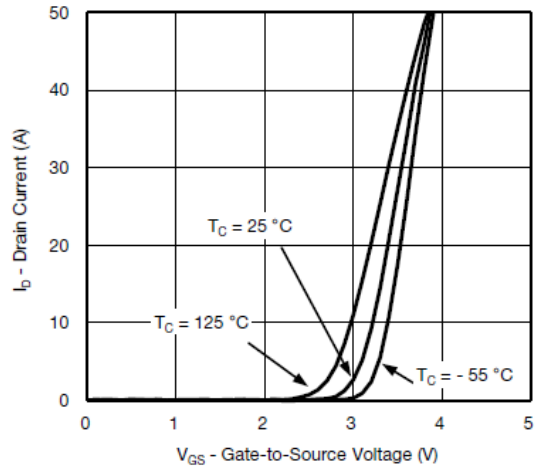
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

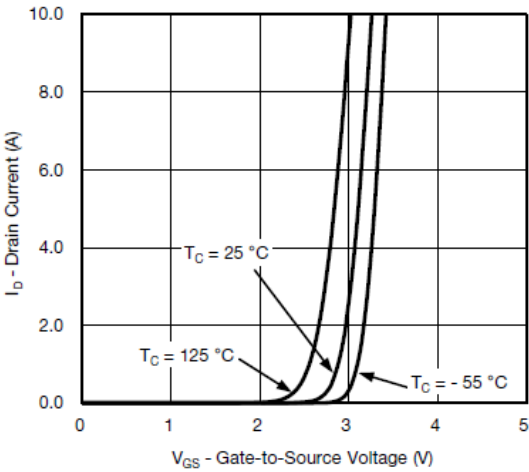
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



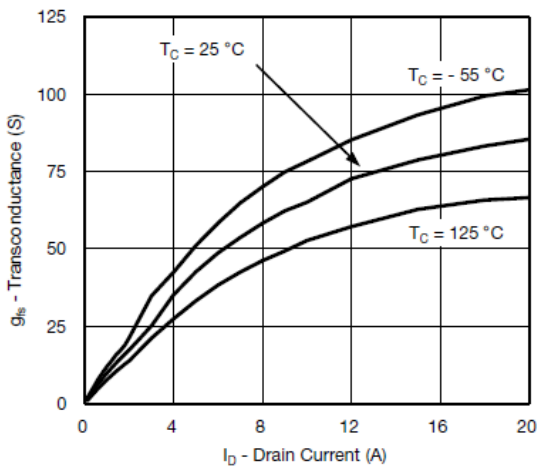
Output Characteristics



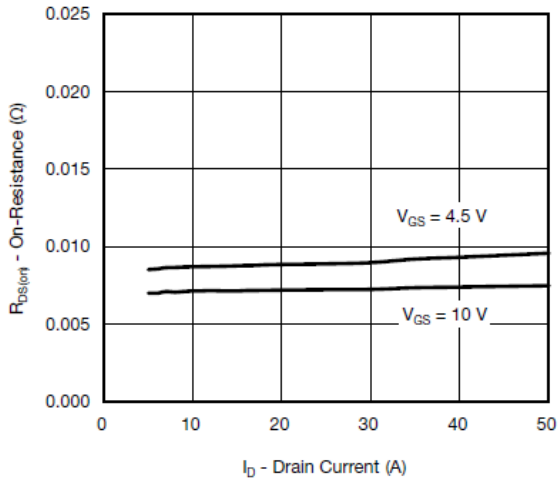
Transfer Characteristics



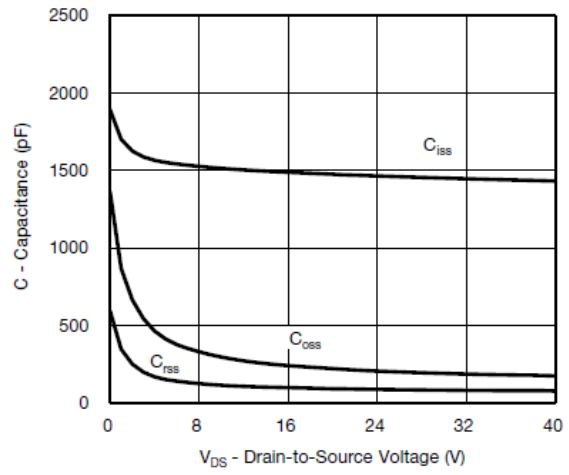
Transfer Characteristics



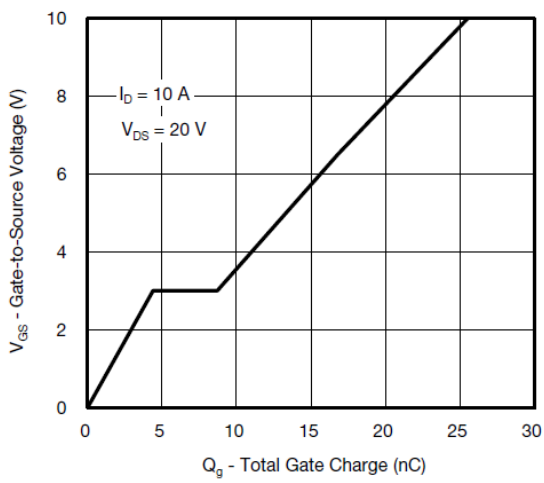
Transconductance



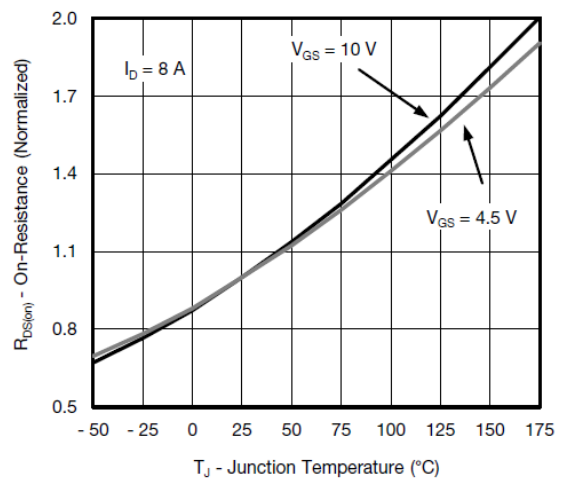
On-Resistance vs. Drain Current



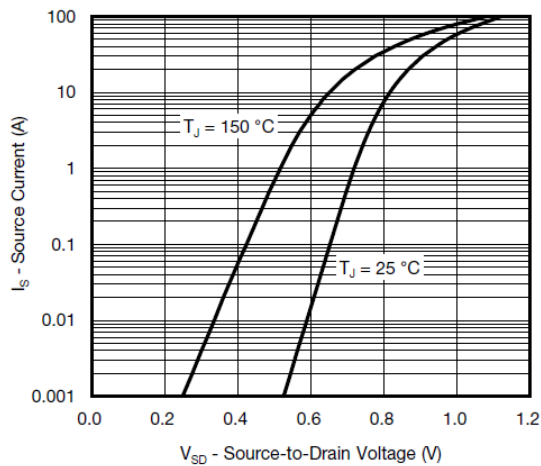
Capacitance



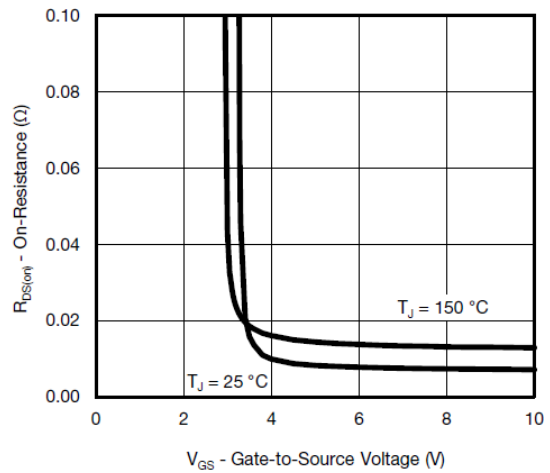
Gate Charge



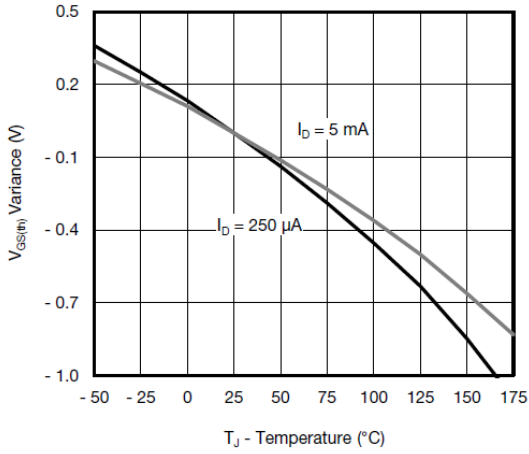
On-Resistance vs. Junction Temperature



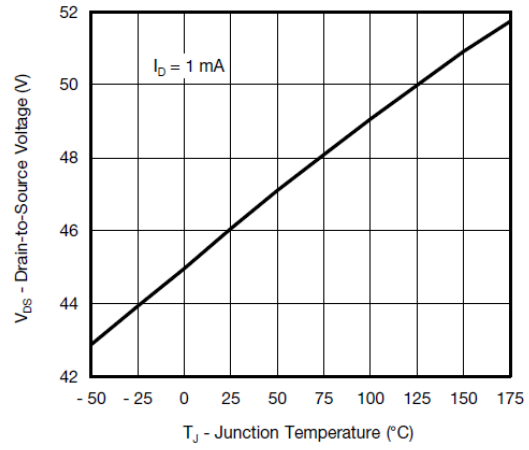
Source Drain Diode Forward Voltage



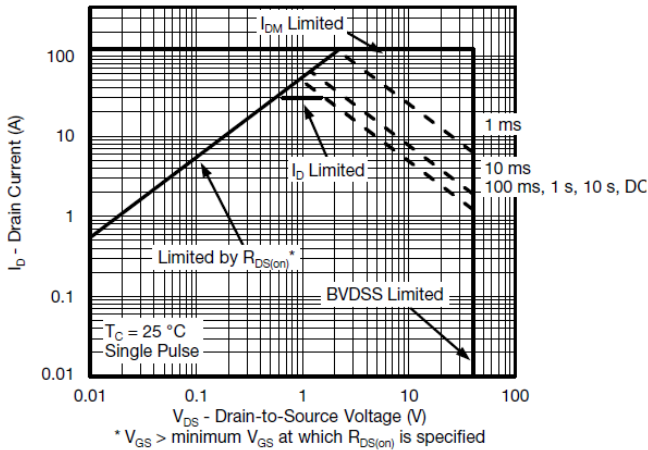
On-Resistance vs. Gate-to-Source Voltage



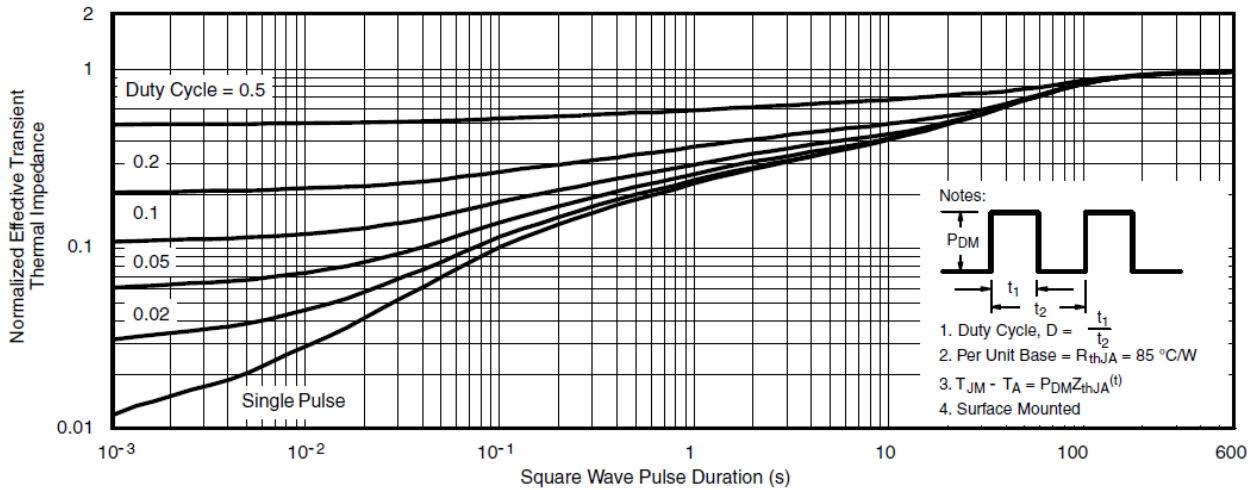
Threshold Voltage



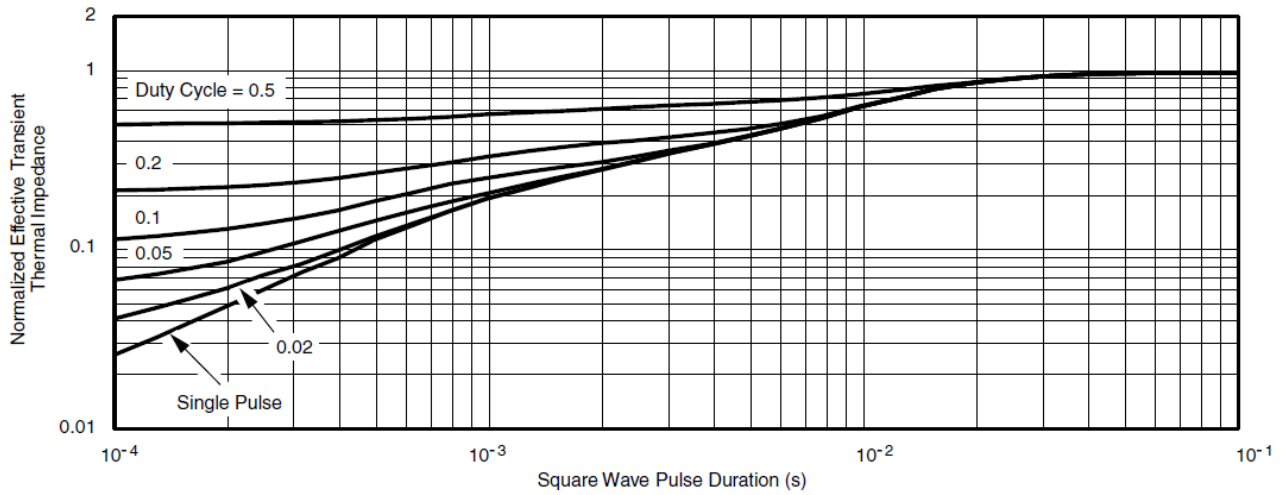
Drain Source Breakdown vs. Junction Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

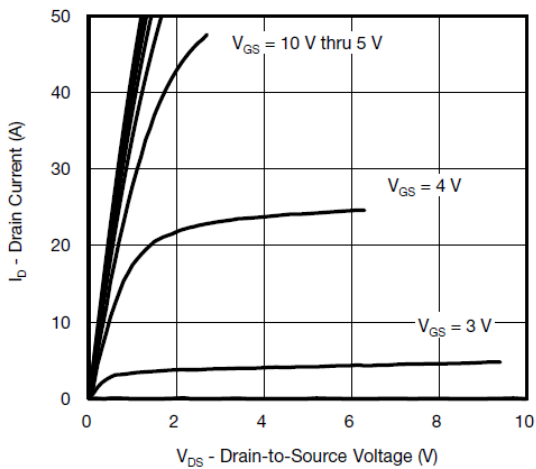


Normalized Thermal Transient Impedance, Junction-to-Case

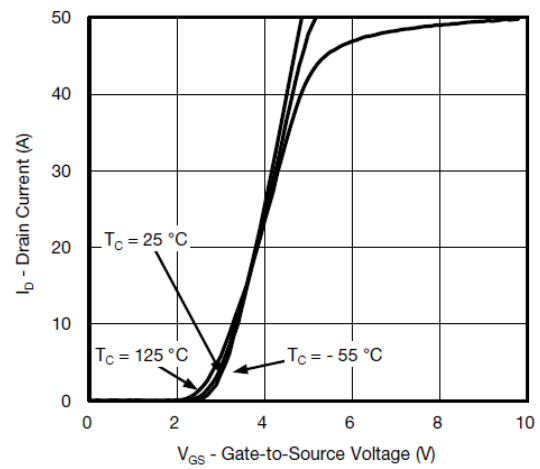
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
- are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

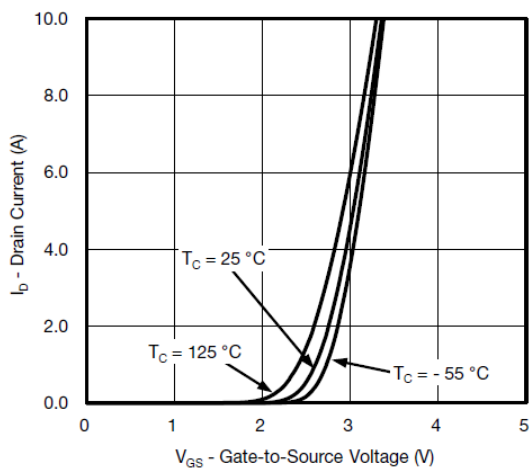
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



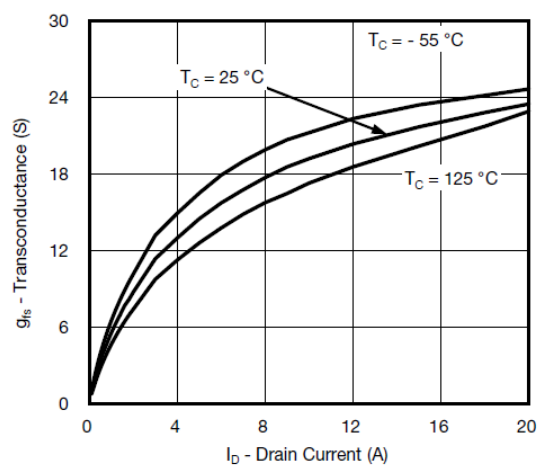
Output Characteristics



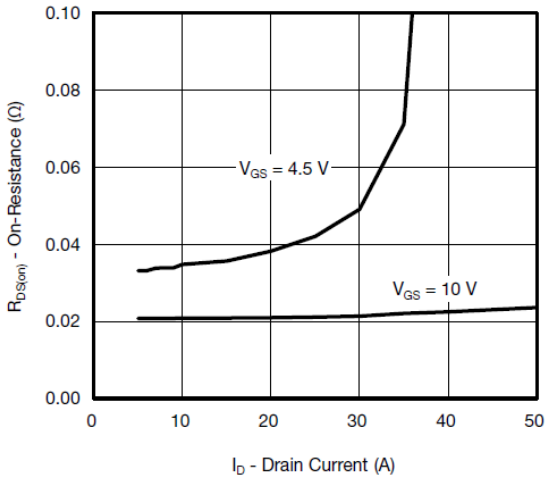
Transfer Characteristics



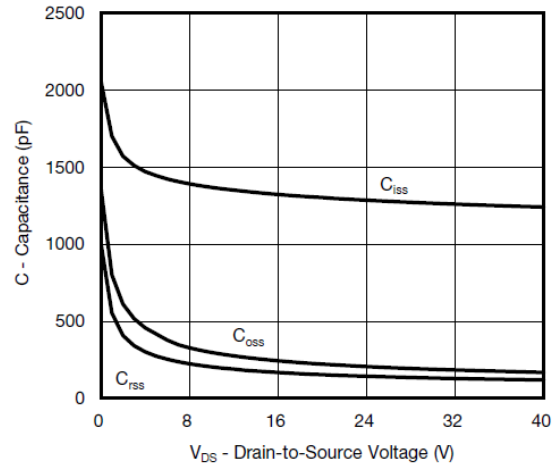
Transfer Characteristics



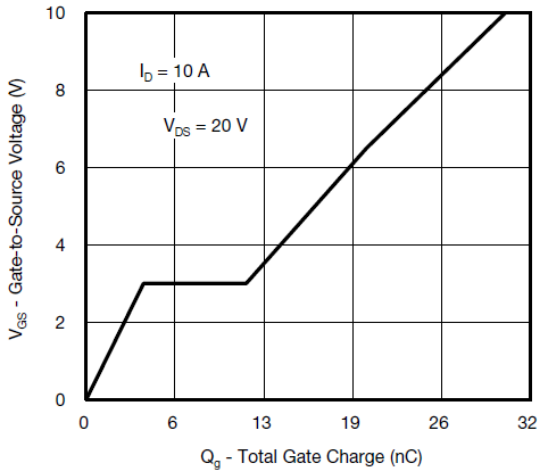
Transconductance



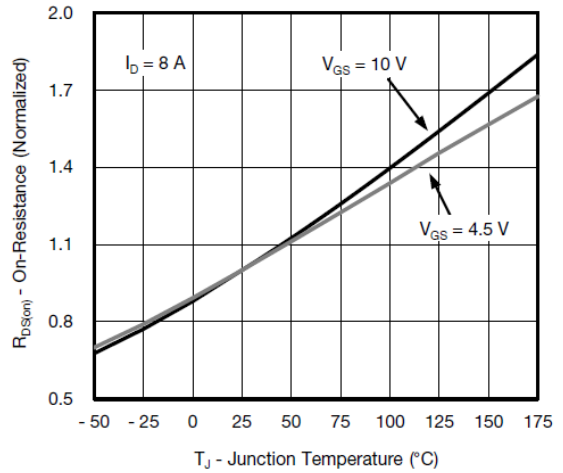
On-Resistance vs. Drain Current



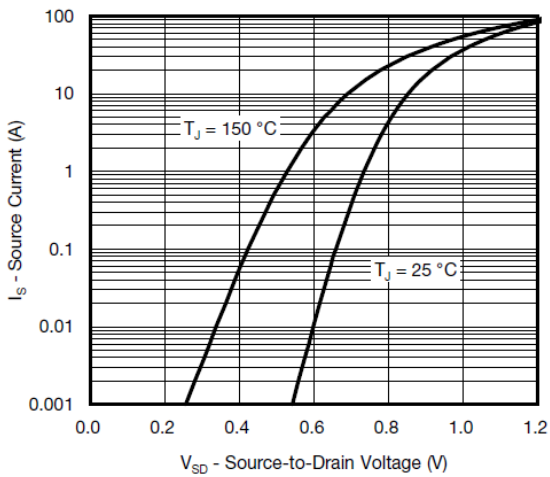
Capacitance



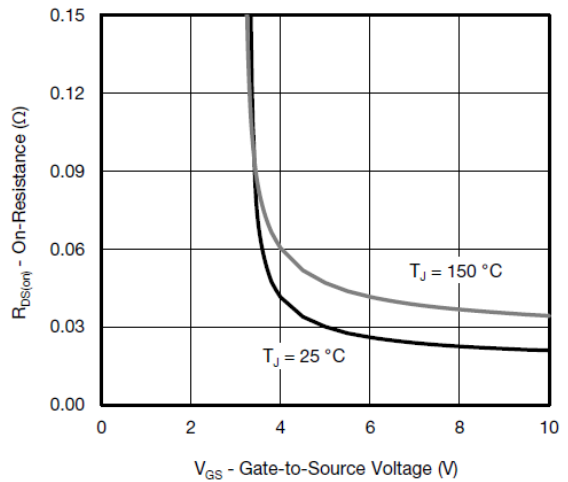
Gate Charge



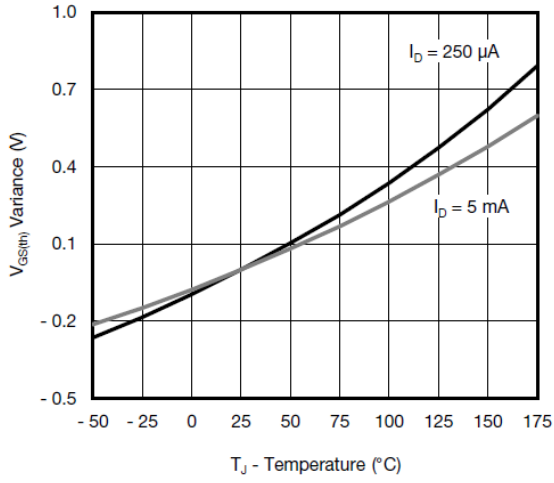
On-Resistance vs. Junction Temperature



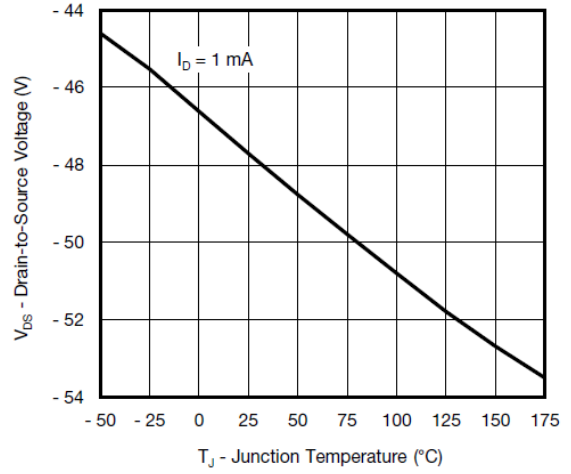
Source Drain Diode Forward Voltage



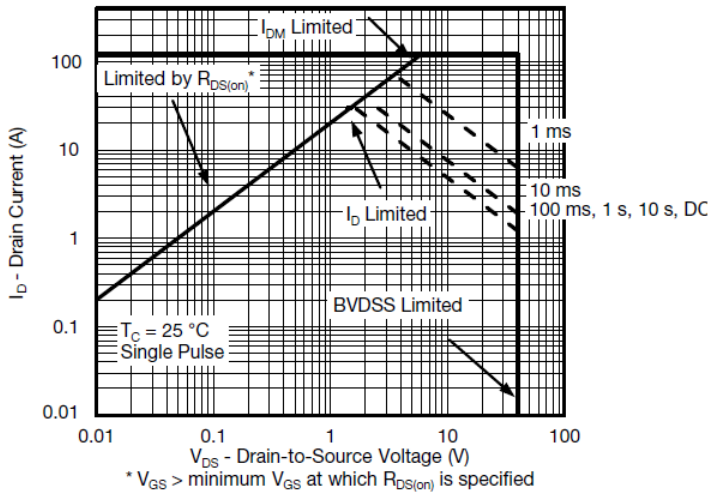
On-Resistance vs. Gate-to-Source Voltage



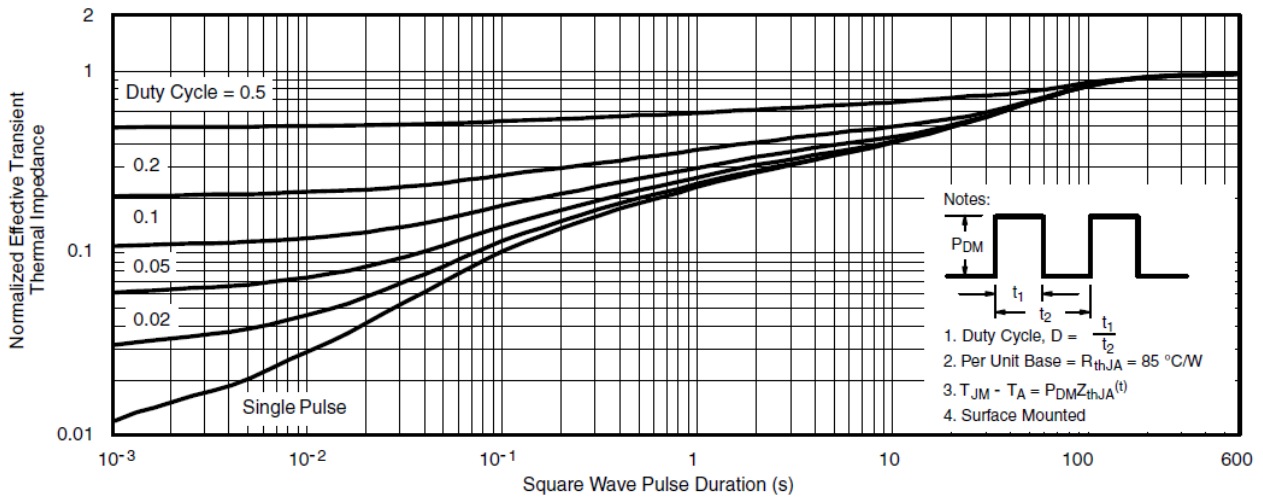
Threshold Voltage



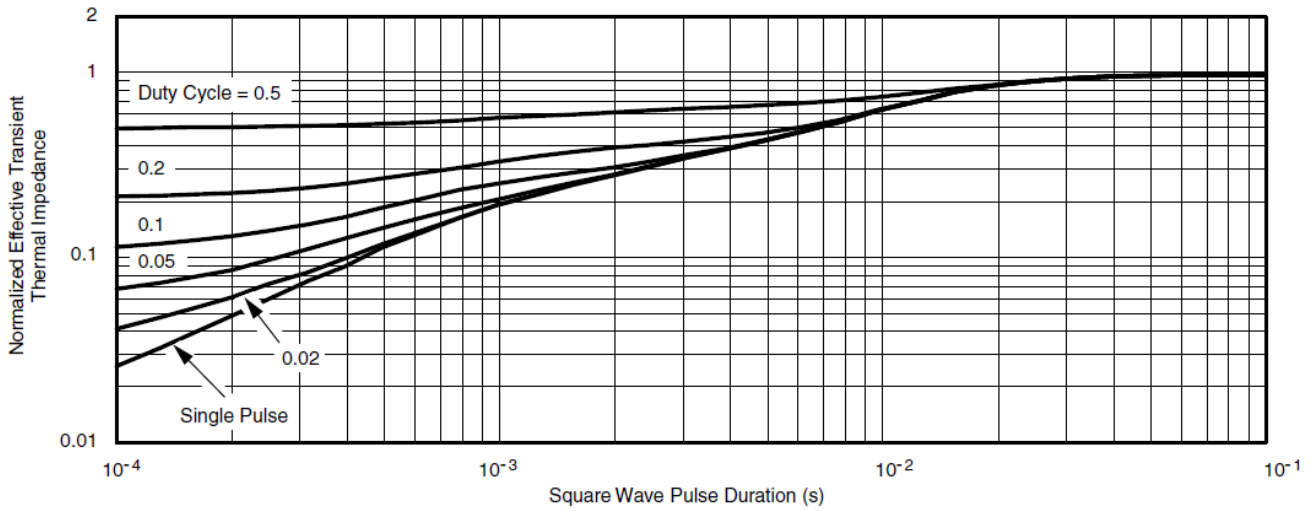
Drain Source Breakdown vs. Junction Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

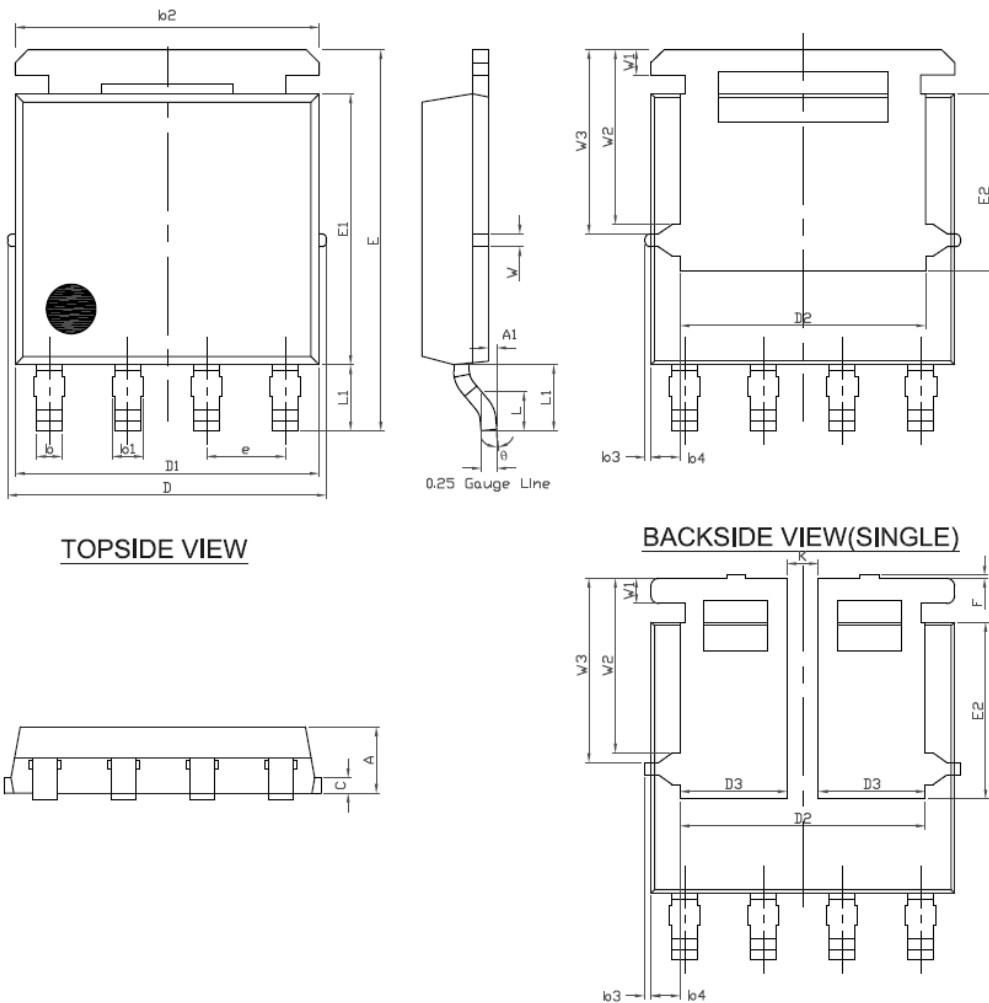


Normalized Thermal Transient Impedance, Junction-to-Case

Note

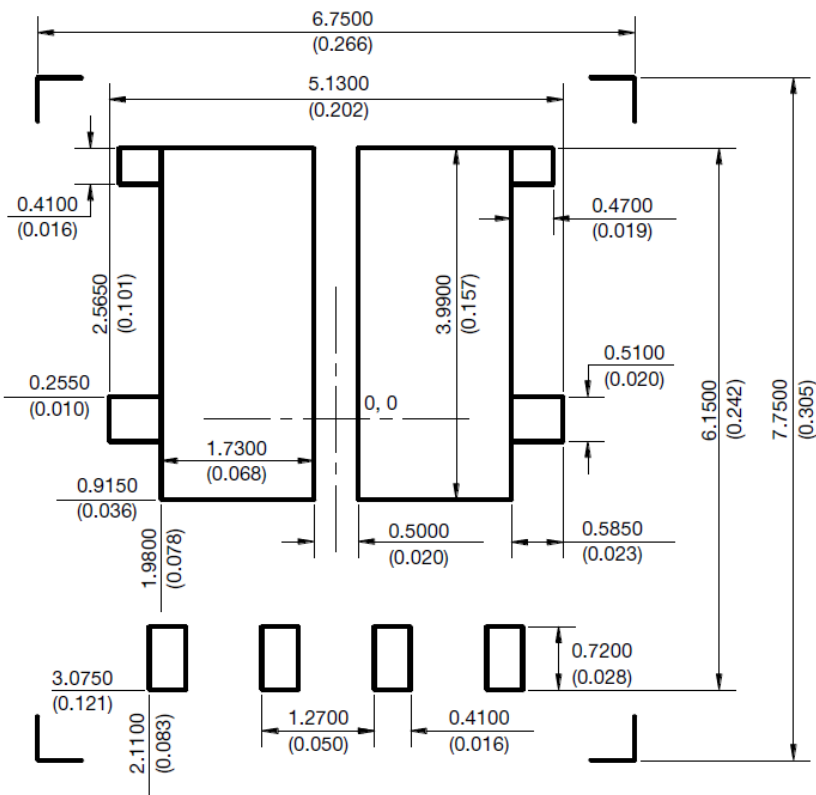
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PDFNWB5x6-8L Package Outline Dimensions



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
q	0°	-	10°	0°	-	10°

RECOMMENDED MINIMUM PAD FOR PDFNWB5x6-8L



Recommended Minimum Pads
Dimensions in mm (inches)
Keep-out 6.75 (0.266) x 7.75 (0.305)

NOTICE

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