



**PDFN/PPAK5\*6-8L Plastic-Encapsulate MOSFETS**

**CCME200N04S N-Channel Power MOSFET**

$V_{(BR)DSS}$	$R_{DS(on)TYP}$	$I_D$
40 V	0.85mΩ@10V	200A

**DESCRIPTION**

The CCME200N04S uses advanced SGT technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications .

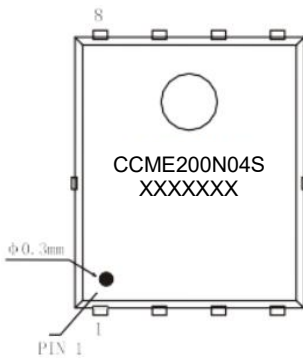
**FEATURES**

- Split Gate Trench Technology
- Low RDS(ON)
- Low Gate Charge
- Low Gate Resistance
- AEC Q101 qualified

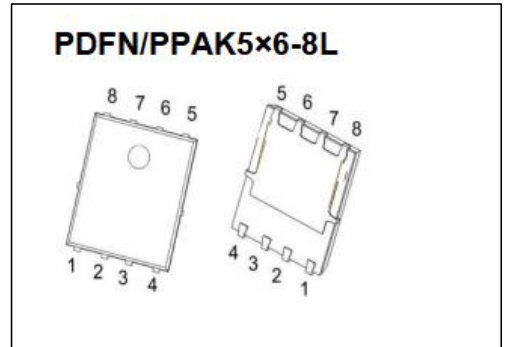
**APPLICATIONS**

- Motors,lamps and solenoid control
- Transmission control
- Power switching application

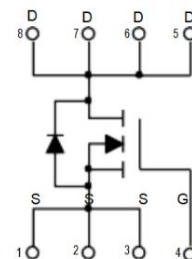
**MARKING**



CCME200N04S =Part No.  
XXXXXXX = Code.



**EQUIVALENT CIRCUIT**



**ABSOLUTE MAXIMUM RATINGS( $T_c=25^{\circ}\text{C}$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>1</sup>	$I_D$	200	A
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	800	A
Single Pulse Avalanche Energy <sup>3</sup>	EAS	1600	mJ
Total Power Dissipation <sup>1</sup>	$P_D$	200	W
Thermal Resistance from Junction to Case <sup>1</sup>	$R_{\theta JC}$	0.75	$^{\circ}\text{C}/\text{W}$
Thermal Resistance from Junction to ambient <sup>4</sup>	$R_{\theta JA}$	48	$^{\circ}\text{C}/\text{W}$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~ +175	$^{\circ}\text{C}$
Soldering Temperature , for 10S(1.6mm from case)	-	260	$^{\circ}\text{C}$

**Notes:**

1. Current is limited by package; with a  $R_{thjc} = 0.75^{\circ}\text{C}/\text{W}$  the chip is able to carry 330 A at  $25^{\circ}\text{C}$ .
2.  $P_W \leq 10\mu\text{s}$ , Duty cycle  $\leq 1\%$ .
3. EAS condition:  $V_{DD}=40\text{V}, V_{GS}=10\text{V}, I_D=80\text{A}, L=0.5\text{mH}, R_g=25\Omega$  Starting  $T_J = 25^{\circ}\text{C}$ .
4.  $6\text{cm}^2$  cooling area. Device on  $40\text{mm} \times 40\text{mm} \times 1.5\text{mm}$  epoxy PCB FR4 with  $6\text{cm}^2$  (one layer, 70um thick) copper area for drain connecting.  
PCB is Vertical in still air.

# MOSFET ELECTRICAL CHARACTERISTICS

TC=25°C unless otherwise specified

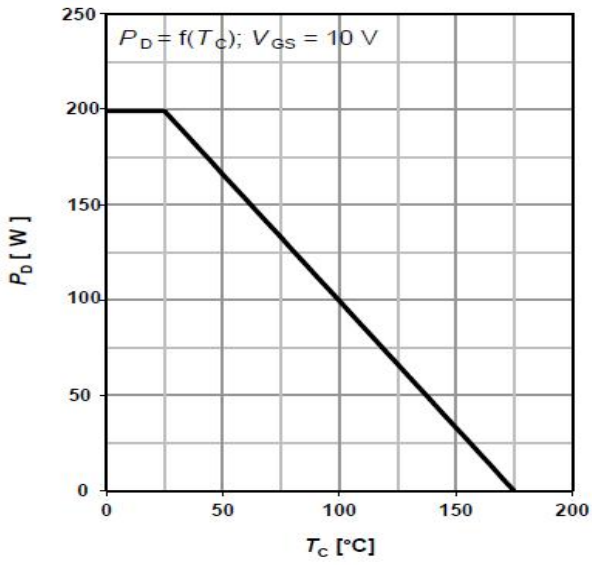
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Off characteristics</b>						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40			V
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 32V, V_{GS} = 0V$			1	$\mu A$
Gate-body leakage current	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$			$\pm 100$	nA
<b>On characteristics<sup>4</sup></b>						
Gate-threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	2.5	4.0	V
Static drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 100A$		0.85	1.0	m $\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = 10V, I_D = 100A$		68		S
<b>Dynamic characteristics<sup>34</sup></b>						
Input capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1MHz$		6714	8050	pF
Output capacitance	$C_{oss}$			1377	1651	
Reverse transfer capacitance	$C_{rss}$			42	62	
Gate resistance	$R_g$	$V_{DS} = 0V, V_{GS} = 0V,$ $f = 1MHz$		1.3		$\Omega$
<b>Switching characteristics<sup>34</sup></b>						
Total gate charge	$Q_g$	$V_{GS} = 0-10V, V_{DD} = 32V,$ $I_D = 200A$		44	58	nC
Gate-source charge	$Q_{gs}$			20	27	
Gate-drain charge	$Q_{gd}$			12	18	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20V, I_D = 200A,$ $V_{GS} = 10V, R_G = 3.5\Omega$		28		ns
Turn-on rise time	$t_r$			26		
Turn-off delay time	$t_{d(off)}$			46		
Turn-off fall time	$t_f$			32		
<b>Drain-Source Diode Characteristics</b>						
Drain-source diode forward voltage <sup>4</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 100A$		0.85	1.2	V
Continuous drain-source diode forward Current <sup>1</sup>	$I_S$	-			200	A
Pulsed drain-source diode forward current <sup>2</sup>	$I_{SM}$	-			800	A
Reverse recovery time	$T_{rr}$	$V_R = 20V, I_F = 50A,$ $di/dt = 100A/\mu s$		50		ns
Reverse recovery charge	$Q_{rr}$			52		nC

Note :

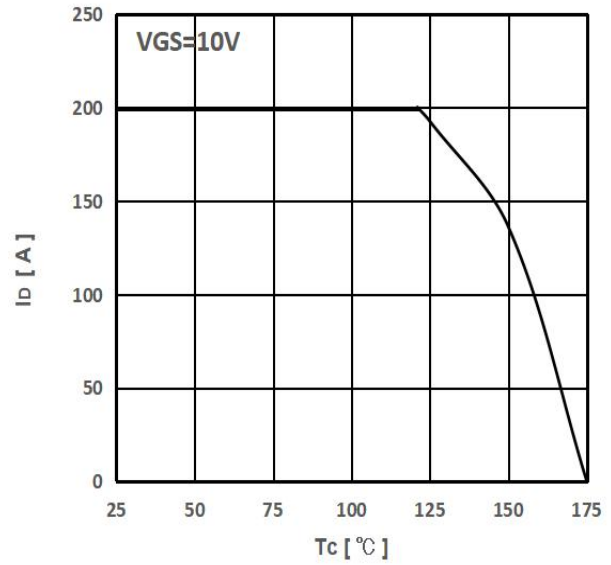
- 1.Current is limited by package; with a  $R_{thjc} = 0.75 \text{ }^\circ\text{C/W}$  the chip is able to carry 330 A at 25°C.
2. $P_w \leq 10\mu s$ , Duty cycle  $\leq 1\%$ .
- 3.Guaranteed by design, not subject to production.
- 4.Pulse Test : Pulse Width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .

# Typical Characteristics

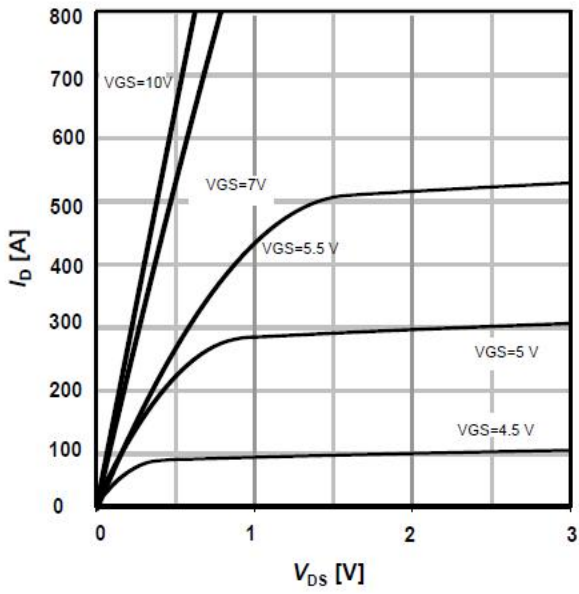
PD -- Tc



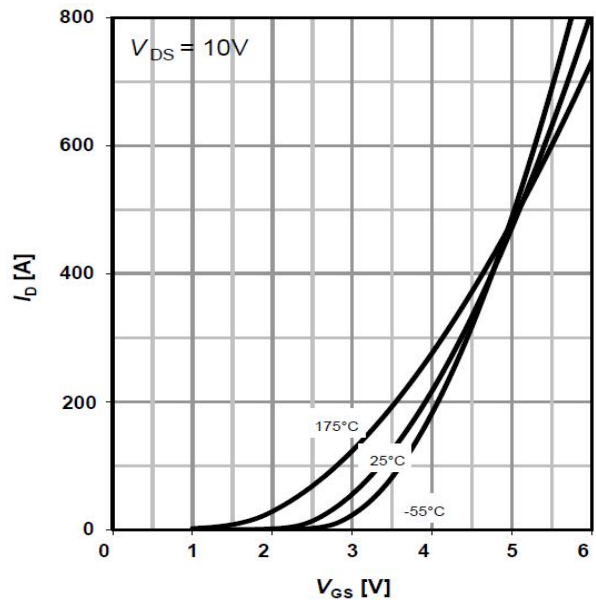
ID -- Tc



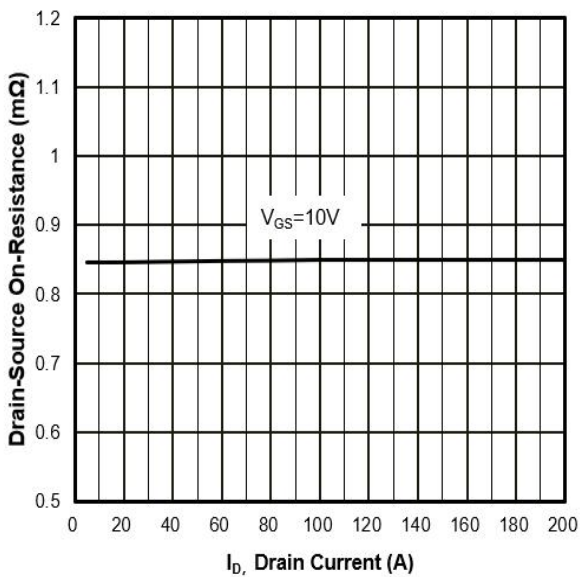
ID -- VDS



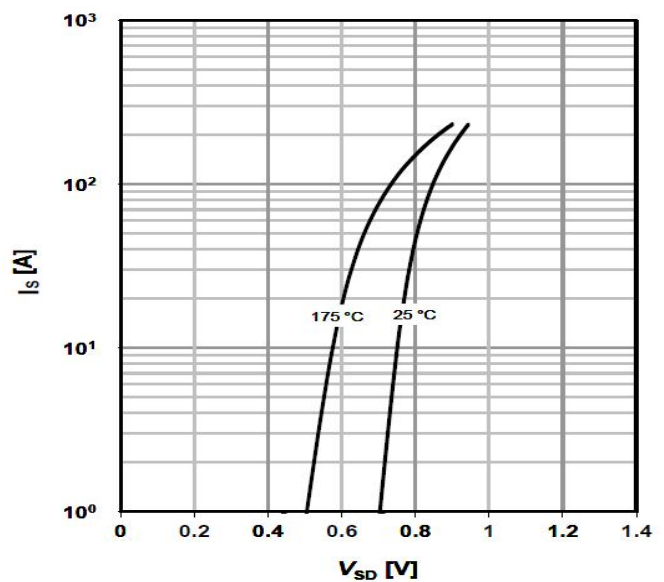
ID -- VGS



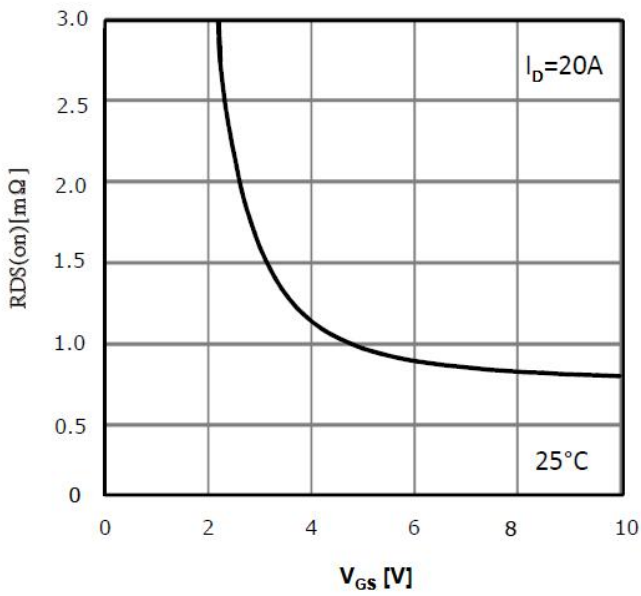
RDS(on) -- ID



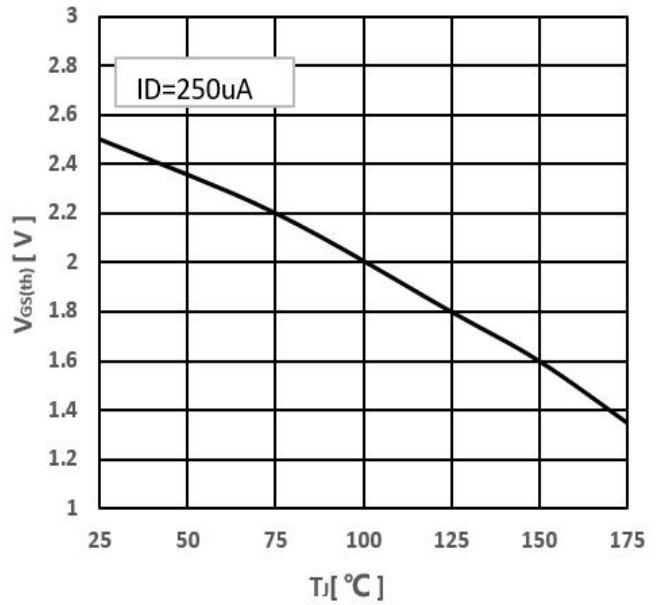
IS -- VSD



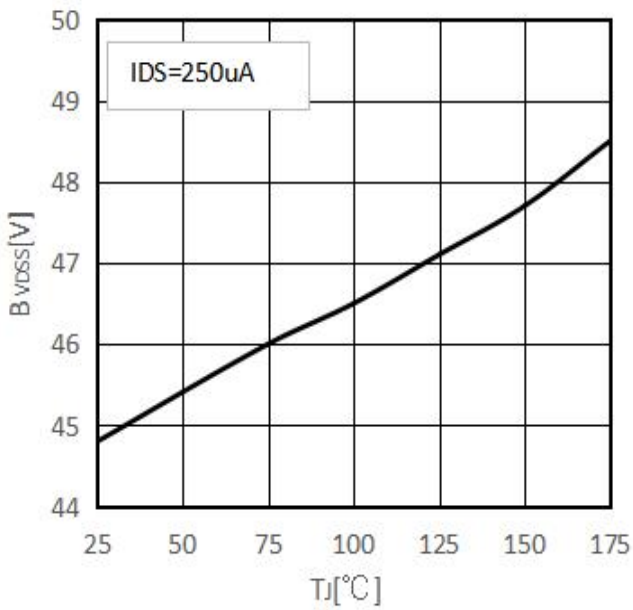
**RDS(on) -- VGS**



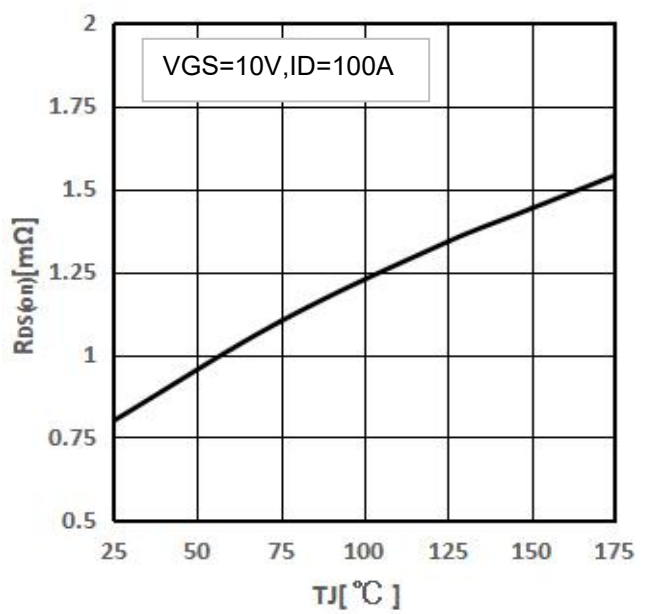
**Threshold Voltage**



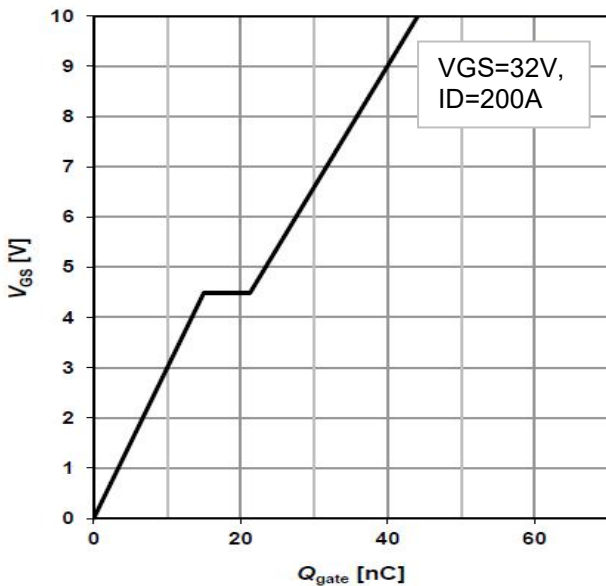
**Drain-source breakdown voltage**



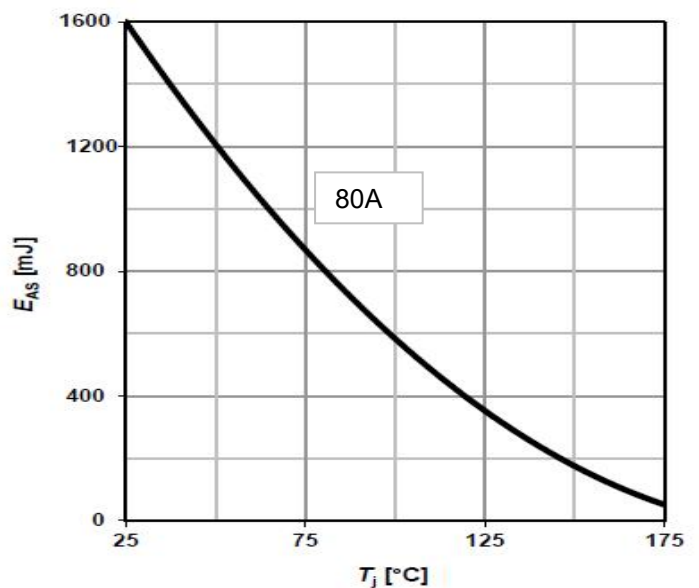
**RDS (on) -- TJ**



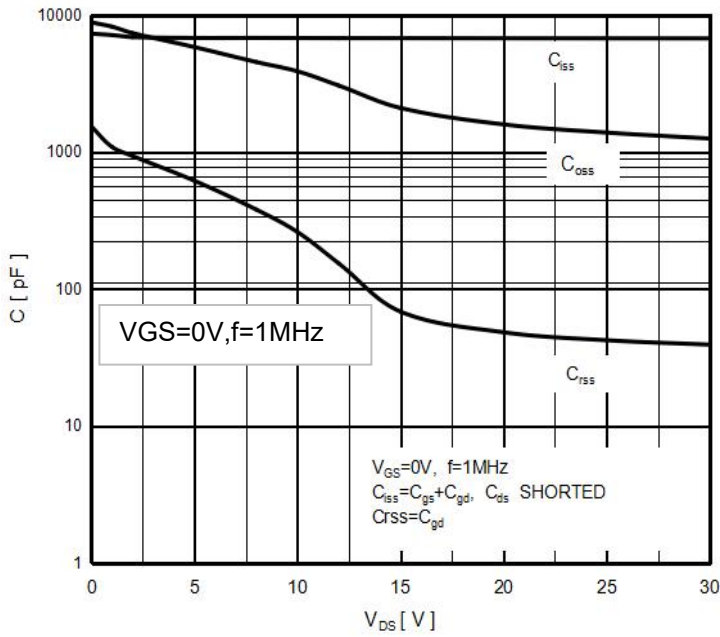
**Typ.gate charge**



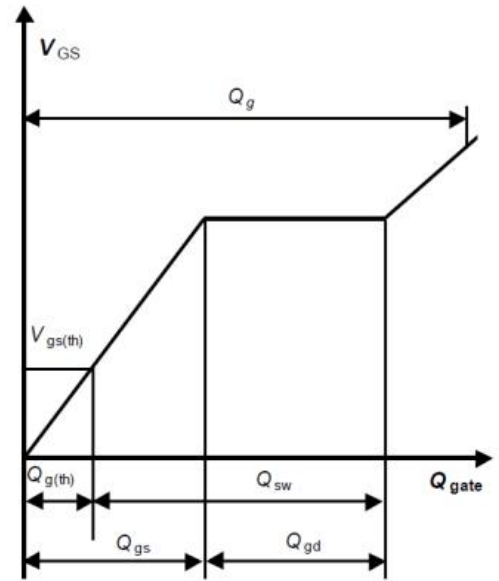
**Avalanche energy**



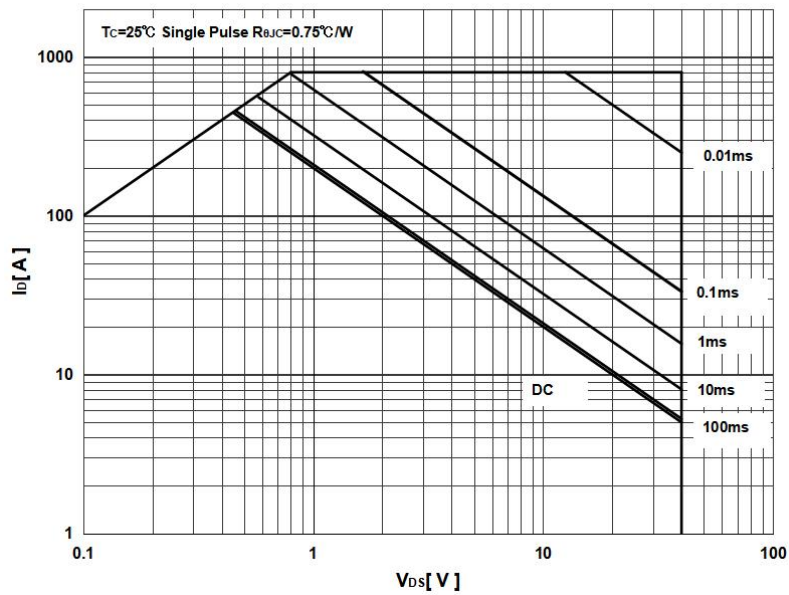
Typ. capacitance



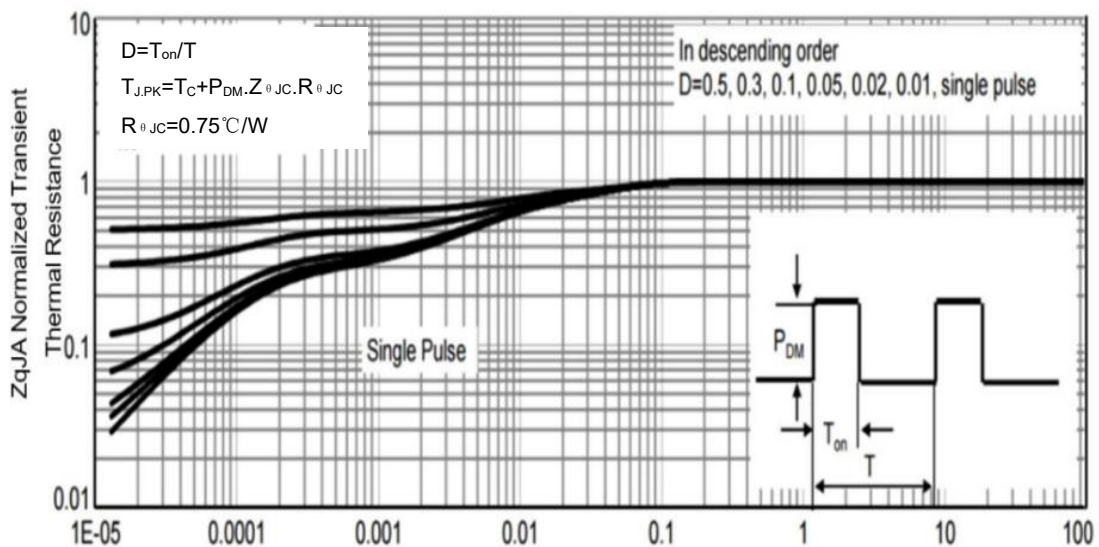
Gate charge waveforms



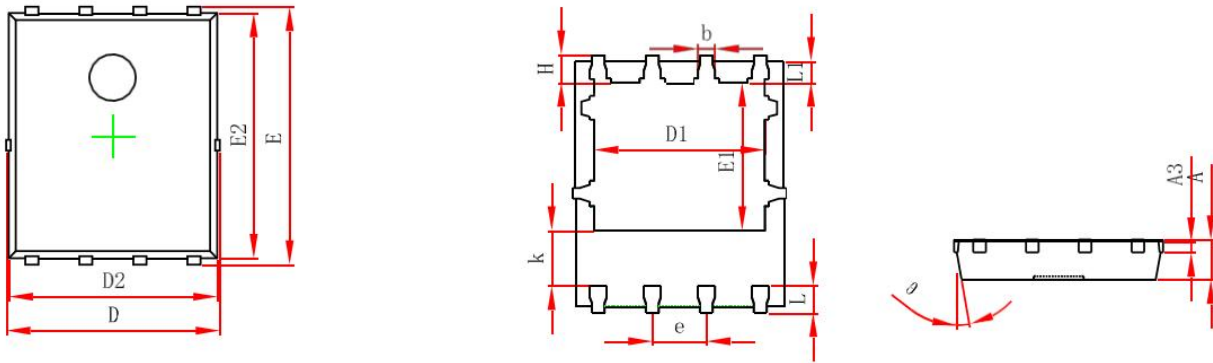
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance

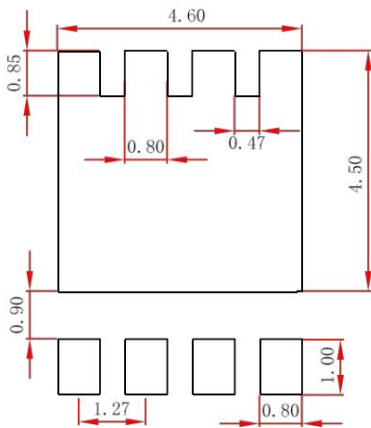


## PDFN/PPAK5\*6-8L Package Outline Dimensions



Symbol	Dimension in Millimeters		Dimension in Inches	
	Min	Max	Min	Max
A	0.950	1.150	0.037	0.045
D	4.950	5.350	0.195	0.211
E	5.950	6.350	0.234	0.250
D1	3.900	4.200	0.154	0.165
E1	3.380	3.730	0.133	0.147
D2	4.900	5.300	0.193	0.209
E2	5.700	5.900	0.224	0.232
k	1.180	1.480	0.046	0.058
b	0.350	0.450	0.014	0.018
e	1.220	1.320	0.048	0.052
L	0.500	0.700	0.020	0.028
L1	0.400	0.575	0.016	0.023
H	0.500	0.700	0.020	0.028
θ	10°	12°	10°	12°

## PDFN/PPAK5\*6-8L Suggested Pad Layout



### Note:

1. Controlling dimension: in millimeters.
2. General tolerance: 0.5mm.
3. The pad layout is for reference purposes only.

### NOTICE

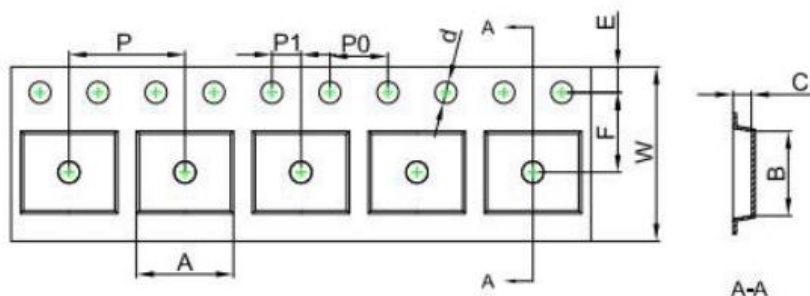
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## PDFN/PPAK5\*6-8L Tape and Reel

### PDFN/PPAK5\*6-8L Embossed Carrier Tape

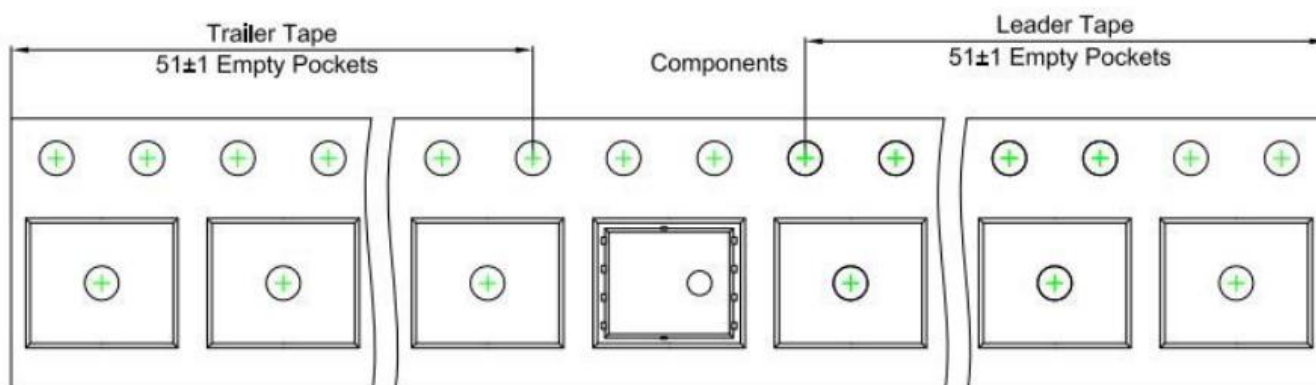


#### Packaging Description:

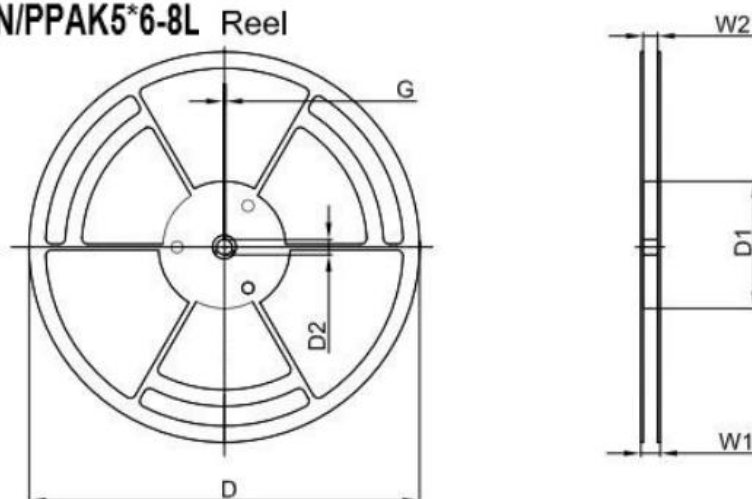
PDFN/PPAK5\*6-8L parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 5,000 units per 13" or 33.0 cm diameter reel. The reels are clear in color and is made of polystyrene plastic (anti-static coated).

Dimensions are in millimeter										
Pkg type	A	B	C	d	E	F	P0	P	P1	W
PDFN/PPAK5*6-8L	6.30	5.30	1.10	Ø1.50	1.75	5.50	4.00	8.00	2.00	12.00

### PDFN/PPAK5\*6-8L Tape Leader and Trailer



### PDFN/PPAK5\*6-8L Reel



Dimensions are in millimeter						
Reel Option	D	D1	D2	G	W1	W2
13"D1a	Ø330.00	100.00	13.00	1.90	17.60	12.40

REEL	Reel Size	Box	Box Size(mm)	Carton	Carton Size(mm)
5,000 pcs	13 inch	5,000 pcs	340×336×29	50,000 pcs	353×346×365



Date of change	Rev #	revise content
2022/12/12	A/0	/
2023/05/16	A/1	产品升级
2023/10/19	A/2	微调产品实测参数（提高测试电流），增加结电容上限